FUSE BOX OF SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

## ABSTRACT OF THE DISCLOSURE

A fuse box includes a semiconductor substrate having a fuse region, and a lower line in the fuse region that has a first region and a second region. An upper line is placed on the upper part of the lower line to overlap the first region. A fuse is placed on the upper part of the upper line, and connects electrically to the second region of the lower line and the upper surface of the upper line. A lower interlayer insulating layer is interposed between the lower line and the upper line, and an upper interlayer insulating layer is interposed between the upper line and the fuse. The fuse is formed on the upper interlayer insulating layer. Both ends of the fuse connect electrically to the second region of the lower line and the upper line, respectively, through fuse holes penetrating the lower and upper interlayer insulating layers.